Administrator: Eingabeaufforderung

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Coreinfo v3.31 - Dump information on system CPU and memory topology
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Intel(R) Core(TM)2 Duo CPU     E6850  @ 3.00GHz
x86 Family 6 Model 15 Stepping 11, GenuineIntel
Microcode signature: 000000B6
HTT                 *       Hyperthreading enabled
HYPERVISOR          -       Hypervisor is present
VMX                 *       Supports Intel hardware-assisted virtualization
SVM                 -       Supports AMD hardware-assisted virtualization
X64                 *       Supports 64-bit mode

SMX                 *       Supports Intel trusted execution
SKINIT              -       Supports AMD SKINIT

NX                  *       Supports no-execute page protection
SMEP                -       Supports Supervisor Mode Execution Prevention
SMAP                -       Supports Supervisor Mode Access Prevention
PAGE1GB             -       Supports 1 GB large pages
PAE                 *       Supports > 32-bit physical addresses
PAT                 *       Supports Page Attribute Table
PSE                 *       Supports 4 MB pages
PSE36               *       Supports > 32-bit address 4 MB pages
PGE                 *       Supports global bit in page tables
SS                  *       Supports bus snooping for cache operations
VME                 *       Supports Virtual-8086 mode
RDWRFSGSBASE        -       Supports direct GS/FS base access

FPU                 *       Implements i387 floating point instructions
MMX                 *       Supports MMX instruction set
MMXEXT              -       Implements AMD MMX extensions
3DNOW               -       Supports 3DNow! instructions
3DNOWEXT            -       Supports 3DNow! extension instructions
SSE                 *       Supports Streaming SIMD Extensions
SSE2                *       Supports Streaming SIMD Extensions 2
SSE3                *       Supports Streaming SIMD Extensions 3
SSSE3               *       Supports Supplemental SIMD Extensions 3
SSE4a               -       Supports Streaming SIMDR Extensions 4a
SSE4.1              -       Supports Streaming SIMD Extensions 4.1
SSE4.2              -       Supports Streaming SIMD Extensions 4.2

AES                 -       Supports AES extensions
AVX                 -       Supports AVX intruction extensions
FMA                 -       Supports FMA extensions using YMM state
MSR                 *       Implements RDMSR/WRMSR instructions
MTRR                *       Supports Memory Type Range Registers
XSAVE               -       Supports XSAVE/XRSTOR instructions
OSXSAVE             -       Supports XSETBV/XGETBV instructions
RDRAND              -       Supports RDRAND instruction
RDSEED              -       Supports RDSEED instruction

CMOV                *       Supports CMOVcc instruction
CLFSH               *       Supports CLFLUSH instruction
CX8                 *       Supports compare and exchange 8-byte instructions
CX16                *       Supports CMPXCHG16B instruction
BMI1                -       Supports bit manipulation extensions 1
BMI2                -       Supports bit manipulation extensions 2
ADX                 -       Supports ADCX/ADOX instructions
DCA                 -       Supports prefetch from memory-mapped device
F16C                -       Supports half-precision instruction
FXSR                *       Supports FXSAVE/FXSTOR instructions
FFXSR               -       Supports optimized FXSAVE/FSRSTOR instruction
MONITOR             *       Supports MONITOR and MWAIT instructions
MOVBE               -       Supports MOVBE instruction
ERMSB               -       Supports Enhanced REP MOVSB/STOSB
PCLMULDQ            -       Supports PCLMULDQ instruction
POPCNT              -       Supports POPCNT instruction
LZCNT               -       Supports LZCNT instruction
SEP                 *       Supports fast system call instructions
LAHF-SAHF           *       Supports LAHF/SAHF instructions in 64-bit mode
HLE                 -       Supports Hardware Lock Elision instructions
RTM                 -       Supports Restricted Transactional Memory instructions

DE                  *       Supports I/O breakpoints including CR4.DE
DTES64              *       Can write history of 64-bit branch addresses
DS                  *       Implements memory-resident debug buffer
DS-CPL              *       Supports Debug Store feature with CPL
PCID                -       Supports PCIDs and settable CR4.PCIDE
INVPCID             -       Supports INVPCID instruction
PDCM                *       Supports Performance Capabilities MSR
RDTSCP              -       Supports RDTSCP instruction
TSC                 *       Supports RDTSC instruction
TSC-DEADLINE        -       Local APIC supports one-shot deadline timer
TSC-INVARIANT       -       TSC runs at constant rate
xTPR                *       Supports disabling task priority messages

EIST                *       Supports Enhanced Intel Speedstep
ACPI                *       Implements MSR for power management
TM                  *       Implements thermal monitor circuitry
TM2                 *       Implements Thermal Monitor 2 control
APIC                *       Implements software-accessible local APIC
x2APIC              -       Supports x2APIC

CNXT-ID             -       L1 data cache mode adaptive or BIOS

MCE                 *       Supports Machine Check, INT18 and CR4.MCE
MCA                 *       Implements Machine Check Architecture
PBE                 *       Supports use of FERR#/PBE# pin

PSN                 -       Implements 96-bit processor serial number

PREFETCHW           *       Supports PREFETCHW instruction

Maximum implemented CPUID leaves: 0000000A (Basic), 80000008 (Extended).

Logical to Physical Processor Map:
*-  Physical Processor 0
-*  Physical Processor 1

Logical Processor to Socket Map:
**  Socket 0

Logical Processor to NUMA Node Map:
**  NUMA Node 0

No NUMA nodes.

Logical Processor to Cache Map:
*-  Data Cache          0, Level 1,   32 KB, Assoc   8, LineSize  64
*-  Instruction Cache   0, Level 1,   32 KB, Assoc   8, LineSize  64
-*  Data Cache          1, Level 1,   32 KB, Assoc   8, LineSize  64
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